

## Research Article

# Development of Combinatorial Pulsed Laser Deposition for Expedited Device Optimization in CdTe/CdS Thin-Film Solar Cells

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A combinatorial pulsed laser deposition system was developed by integrating a computer controlled scanning sample stage in order to rapidly screen processing conditions relevant to CdTe/CdS thin-film solar cells. Using this system, the thickness of the CdTe absorber layer is varied across a single sample from 1.5  $\mu\text{m}$  to 0.75  $\mu\text{m}$ . The effects of thickness on CdTe grain morphology, crystal orientation, and cell efficiency were investigated with respect to different postprocessing conditions. It is shown that the thinner CdTe layer of 0.75  $\mu\text{m}$  obtained the best power conversion efficiency up to 5.3%. The results of this work shows the importance that CdTe grain size/morphology relative to CdTe thickness has on device performance and quantitatively exhibits what those values should be to obtain efficient thin-film CdTe/CdS solar cells fabricated with pulsed laser deposition. Further development of this combinatorial approach could enable high-throughput exploration and optimization of CdTe/CdS solar cells.

## 1. Introduction

CdTe solar cells have shown great promise in competing with Si solar cells, which currently dominate the photovoltaic (PV) market. CdTe solar cells have a higher theoretical limiting efficiency than Si solar cells due to CdTe's nearly optimal band gap for our Sun and high absorption coefficient [1–4]. Recent improvements seen in CdTe solar cells make it reasonable for CdTe to take over a significant portion of the PV market [5]. However, the champion CdTe cells for power conversion efficiency have all been thick film (~5–8  $\mu\text{m}$ ) devices. If these kinds of cells are manufactured on a large scale the cost will eventually increase significantly considering the limited amount of Te available. As such, recent research has been focused on thin-film CdTe solar cells (~1  $\mu\text{m}$ ), which in addition to protecting Te reserves would reduce the overall material cost of device fabrication. Altering the structural parameters of these thin-film cells, in addition

to the compositional and postprocessing parameters, can easily lengthen and complicate the optimization process. Therefore, these conditions are typically optimized with respect to a specific thickness which conventionally calls for many separate samples to be fabricated.

Combinatorial processing and characterization are the method of producing a sample with varied material properties across a single sample [6]. This effectively allows a continuum of device performances to be measured as a function of the varied property with a single sample. Combinatorial pulsed laser deposition (cPLD) has been used before to vary chemical compositions across C-MOS transistors, for example, [6]. PLD is a relatively new fabrication technique applied for CdTe solar cells. While its application to solar cells has proven effective in past research, a systematic study of the effect of the PLD processing conditions is lacking [7, 8]. PLD is advantageous for thin-film depositions due to its highly controllable deposition rate and also its many easily

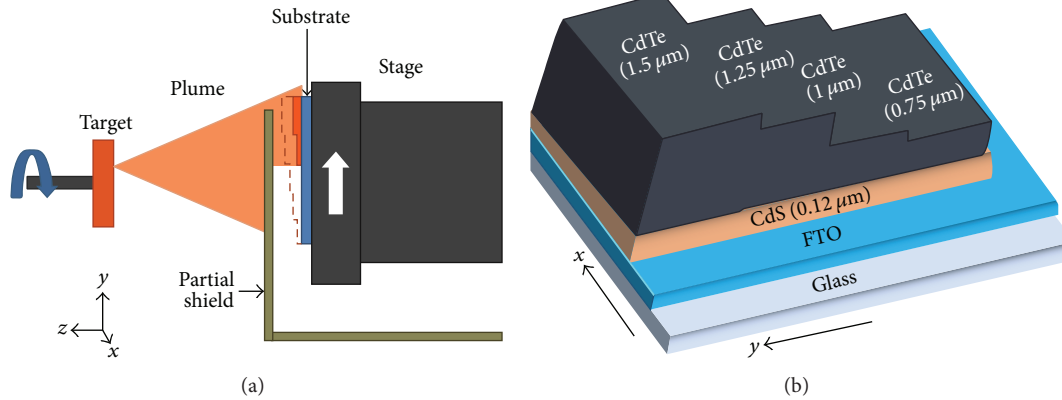


FIGURE 1: A depiction of the combinatorial PLD process which allows different thicknesses to be deposited on a single substrate (a) and a schematic drawing of the samples made with varying CdTe thickness (b).

adjustable ablation parameters including laser repetition rate, pulse length, energy density, target-substrate distance, and chamber atmosphere and temperature [9]. In combinatorial PLD fabrication of CdS/CdTe thin-film solar cells, additional advantages are provided in generating different device structures for expedited optimization of the device performance.

In thin-film CdS/CdTe solar cells, the CdTe grain size and microstructure relative to its thickness are extremely important to device performance. In order to investigate the effects of CdTe thickness on CdTe microstructure and cell performance and establish a method of probing for device optimization, a programmable scanning sample stage was implemented into the PLD system for combinatorial fabrication of CdTe. In particular, this work analyzed the properties of cPLD made CdTe and studied cell performance when varying the CdTe thickness (1.5, 1.25, 1, and 0.75 μm) on the same sample. A reference sample (denoted in this work by sample A) was fabricated without the typical CdCl<sub>2</sub> annealing treatment and tested to extract the effect of the annealing on the microstructure and crystallinity of CdTe and the resulting CdS/CdTe cell performance. It is demonstrated that the PLD conditions used in this work result in the highest efficiency being obtained by the thinnest CdTe layer of 0.75 μm with an overall maximum efficiency of 5.3%.

## 2. Experimental Method

The PLD system consists of a 248 nm KrF excimer laser from Lambda Physik with a 20 ns laser pulse duration. The absorber and window layer targets are mounted inside a vacuum chamber on rotating stands that allow for both targets to be moved into the path of the laser and rotation about the axis of the targets facilitates uniform ablation of the target surface [7, 8, 10–12]. The CdS and CdTe targets were obtained from ACI Alloys and had a 99.99% purity. The substrate stage was mounted into the chamber across from the targets with a distance of 5.5 cm separating the two. The scanning stage has two axes of movement and it can move in any motion desired that is perpendicular to the laser plume axis. Two external stepper motors drive the stage under computer control. The computer control is achieved

by a custom computer program which makes it possible for the stage to undergo very complicated motions. Located in the path of the ablated laser plume, in between the target and substrate, is a partial shield that covers half of the stage when the stage is in its neutral position. This allows for precise control over which area of the substrate is deposited on, granting a combinatorial way to control in situ thickness variations on a single substrate. As the substrate was moved in the y-direction to make the different CdTe thicknesses it was also constantly scanning in the x-direction (in and out of the page in Figure 1(a)) to achieve uniform thickness across the entire substrate. All vacuum and stage equipment is custom and home-built. Thicknesses of 1.5, 1.25, 1.0, and 0.75 μm were chosen to be deposited on top of the 120 nm thick CdS window layer. A depiction of the cPLD setup and the solar cell design is shown in Figure 1.

TEC 15 (from Pilkington North America) soda lime glass, which has a fluorine-doped tin oxide layer with a sheet resistance of 15 Ω/□, was used as the conductive substrate and serves as the front contact to the devices. Before any deposition the substrates were thoroughly cleaned by first a boiling in deionized (DI) water followed by sonication in DI water, acetone, and IPA for 5 minutes each. The CdS window layer was heated to 200°C with the sample stage heater and deposited at this temperature in 1.5 mTorr of Argon gas flow with a laser repetition rate of 10 Hz, spot size of 8.7 mm<sup>2</sup>, and pulse energy of 150 mJ with a 0.3 OD filter reducing the energy to 70 mJ. The CdTe absorber layer parameters are identical except the laser spot size is decreased to 7.6 mm<sup>2</sup> and the thickness is varied in 250 nm steps from 750 nm to 1500 nm using the partial shield and moving stage. After ablation is complete, the sample was annealed in the vacuum chamber at 400°C for 10 min in 20 Torr Ar and cooled naturally overnight to room temperature.

The CdCl<sub>2</sub> anneal was carried out by placing the samples on top of a piece of glass that had been coated with CdCl<sub>2</sub> by dropping a supersaturated methanol/CdCl<sub>2</sub> solution onto it and letting it dry in air. The sample was kept ~3 mm from the CdCl<sub>2</sub> coated glass during the annealing process which took place in a tube furnace with 100 sccm Ar and 25 sccm O<sub>2</sub> flow at 360°C for varying times. Four different cells were

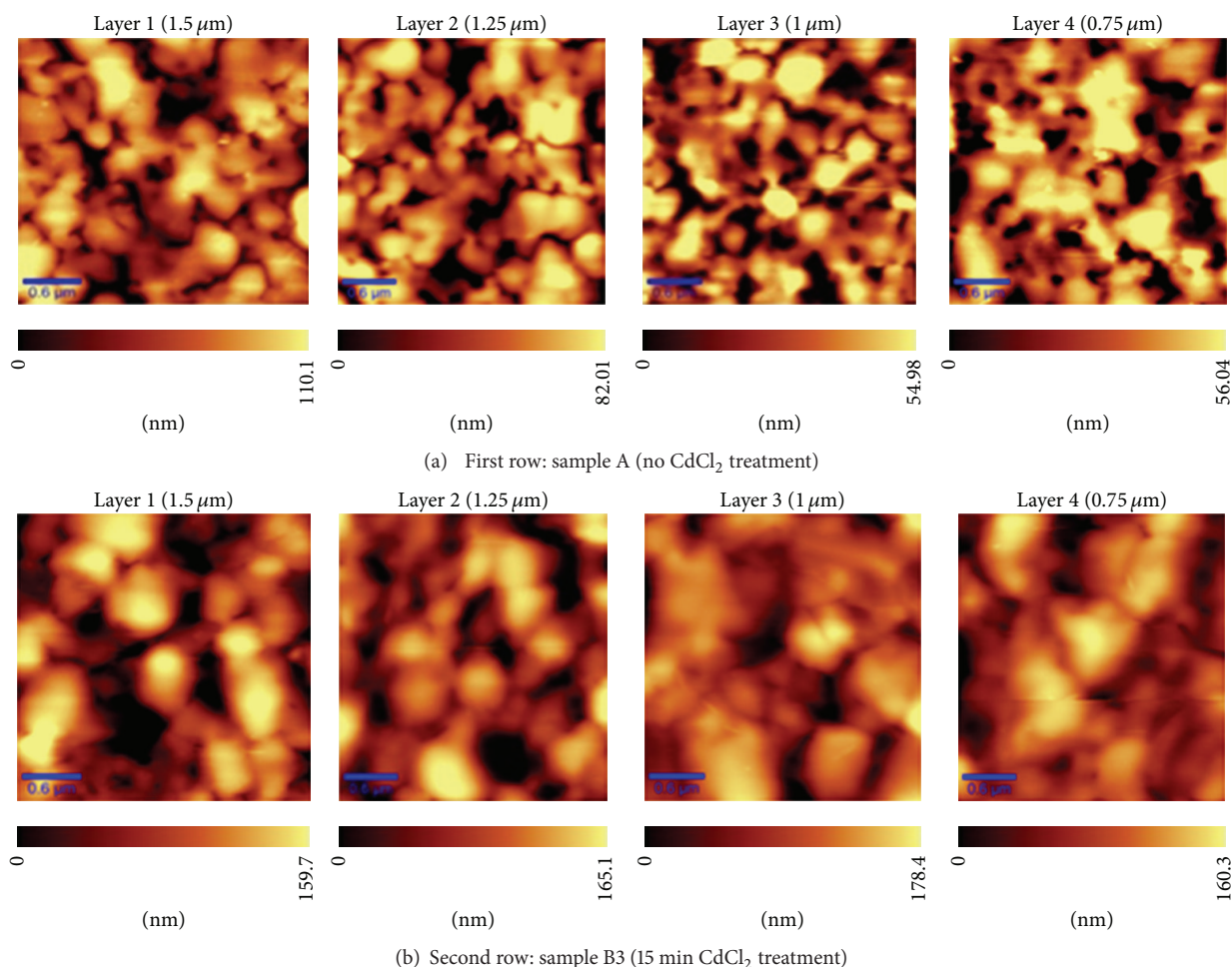


FIGURE 2: First row of AFM images is corresponding to sample A (No  $\text{CdCl}_2$  annealing). The second row is corresponding to the sample B3 (with 15 min  $\text{CdCl}_2$  annealing). The scale bar for all images is  $0.6 \mu\text{m}$ .

made each with a varying  $\text{CdCl}_2$  annealing time of 10, 12, 15, and 17 minutes. These samples are denoted by samples B1, B2, B3, and B4, respectively. All samples were submerged for four seconds in a Bromine etchant produced by mixing 0.2 mL Bromine with 40 mL methanol. The samples were then immediately rinsed with methanol, acetone, and IPA. The etching process is used to remove contaminants from the surface as well as make a Te rich surface for better ohmic contact. A Cu doped HgTe/graphite paste (0.017 g Cu, 4 g HgTe, and 10 g graphite paste) was then made to be applied to the etched CdTe layer as the back contact. Small contacts with average areas of roughly  $1.25 \text{ mm}^2$  are then applied across the entire sample. Four contacts were placed on each layer for device and uniformity testing. After application, the sample is again baked in the tube furnace with 100 sccm Ar flow at  $280^\circ\text{C}$  for 30 minutes. Finally, Ag electrodes were carefully applied to the back contacts with a toothpick and baked in air at  $150^\circ\text{C}$  for 1 hour.

*J-V* characterizations are carried out using a CHI660D electrochemical workstation and a Newport 50–500 W Xenon lamp solar simulator at 1.5 AM ( $100 \text{ mW/cm}^2$ ). The CHI 660D electrochemical workstation and a Newport monochromator were used for external quantum efficiency

(EQE) measurements. Atomic force microscopy (AFM) and Raman spectroscopy (488 nm excitation wavelength) were performed using a WiTec Alpha 300 confocal MicroRaman system to obtain surface roughness and phase orientation for the different growth and annealing conditions.

### 3. Results and Discussion

Atomic force microscopy (AFM) was applied to characterize the CdTe surface morphology. The results are compared in Figure 2 for the CdTe variable thickness sample (sample B3) and the reference sample (sample A), which was fabricated in the same cPLD process but did not experience the  $\text{CdCl}_2$  anneal treatment. Calculations from the AFM analysis software indicate that the average roughness of the CdTe in sample A is in the range of 13–16 nm while, by visual inspection, the CdTe grain size is roughly 140–160 nm. On the other hand, in sample B3, the average roughness for all layers was approximately 30 nm and the grain size is much larger. There is a correlation between the grain size and the thickness of CdTe. This is most easily seen in sample B3 where it is obvious that the grains get bigger as the thickness gets smaller. The thinnest layer of CdTe at  $0.75 \mu\text{m}$  has grains that vary in

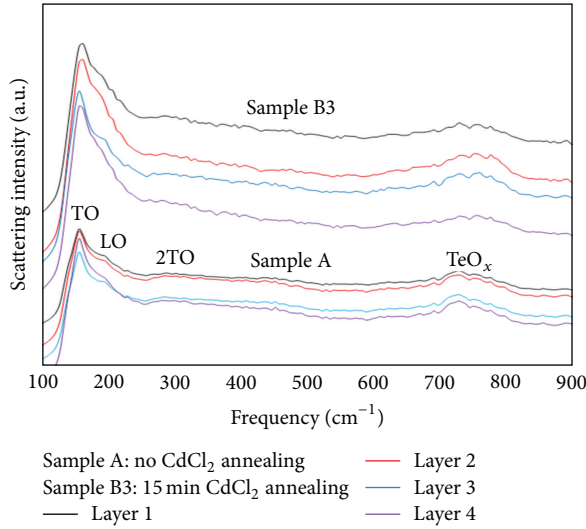


FIGURE 3: The Raman spectra of samples A and B3 before and after the  $\text{CdCl}_2$  treatment.

size from 300 to 700 nm while the thickest layer at  $1.5 \mu\text{m}$  has grains in the range of 150–550 nm. The average grain size for the thinnest layer is approximately 65% of the total thickness. For the thicker layer the average grain size is closer to 20% of the total thickness. This difference seen in grain size per thickness is most likely because the recrystallization is more easily achieved in the thinner layers as there is less material.

Raman spectroscopy was performed in order to examine the structural properties of the different CdTe layers and the data can be seen in Figure 3. The data for each measurement has been shifted on the  $y$ -axis (arbitrary units) for better visibility. The transverse optical phonon mode (TO) for CdTe is known to be located at a Raman shift of  $141 \text{ cm}^{-1}$ , which can clearly be seen in all of the plots. The peak at the  $169 \text{ cm}^{-1}$  shift is assigned to the longitudinal optical phonon (LO) of CdTe [13]. The peaks at  $292 \text{ cm}^{-1}$  and  $750 \text{ cm}^{-1}$  are attributed to the 2TO mode of CdTe and tellurium oxide ( $\text{TeO}_x$ ), respectively [14, 15]. The  $\text{TeO}_x$  signature found in both samples is possibly attributed to oxygen residues which might exist during the fabrication of the samples. The thickness of CdTe appears to have no role on crystal orientation as the Raman spectra between layers of the same sample are nearly identical. The selection rules for CdTe illustrate that the TO and LO modes of CdTe are allowed from (110) and (100), respectively. Also, both modes can be allowed from (111) [16–18]. The LO mode is not highly pronounced in the layers of sample B3 suggesting that the polycrystalline structure is predominantly in the (110) crystal orientation.

Figure 4 shows the  $J$ - $V$  curves that obtained the highest performance for the two samples made with and without  $\text{CdCl}_2$  treatment. The  $JV$  data from sample B3 shows that the best performance came from the thinnest CdTe layer of  $0.75 \mu\text{m}$ . This layer achieved a maximum efficiency of 5.3% with a  $J_{\text{SC}}$ ,  $V_{\text{OC}}$ , and FF of  $17.6 \text{ mA/cm}^2$ ,  $664 \text{ mV}$ , and 46%, respectively. Obviously, with CdTe having an absorption coefficient approaching  $10^5 \text{ cm}^{-1}$  in the visible spectrum, this layer will absorb the fewest photons due to its thickness

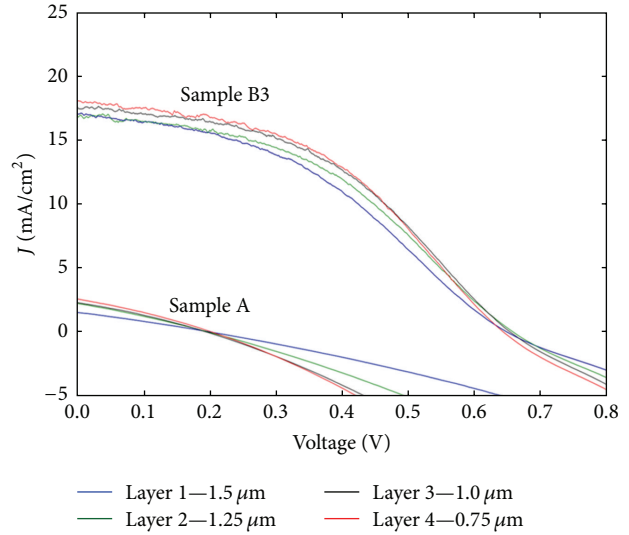


FIGURE 4:  $J$ - $V$  curves for the best performing cells from the two samples made without (A) and with (B3)  $\text{CdCl}_2$  annealing.

in accordance with the Beer-Lambert Law. However, the shortest travel distance for charges to be collected at the electrodes may outweigh the loss in photon absorption as compared to its thicker counterparts. The data from all layers can be seen in Tables 1(a) and 1(b), which contain the average values for the four cells made on each layer. All of the layers in sample A have extremely low performance as expected from its poor crystallinity and unoptimized microstructure. In addition, the extremely small  $V_{\text{OC}}$  is attributed to the weak electric field established by the p-n junction, due to the lack of doping in CdTe which is achieved during the  $\text{CdCl}_2$  annealing process and quite possibly pinhole formation. The CdTe for this sample is possibly nanocrystalline, which causes huge amounts of recombination due to the small grain sizes [19, 20]. This would affect not only the fill factor, but the  $J_{\text{SC}}$  as well. The order of magnitude increase in the  $J_{\text{SC}}$  of sample B3 is due to the increased number of majority carriers, improvements in the grain connectivity, and increases in the grain size, which becomes large enough to eliminate a significant portion of the grain boundaries. However, the rollover seen in sample B3 indicates that there is a Schottky barrier present which occurs due to the mismatch in work function between the CdTe and back contact [21]. Studies are already underway to resolve this issue.

For comparison five total samples were fabricated using cPLD by which the variable thickness of CdTe has been obtained 1.5, 1.25, 1.0, and  $0.75 \mu\text{m}$  in correspondence to layers 1, 2, 3, and 4, respectively, on the same substrate. Sample A regards those not treated with ex situ  $\text{CdCl}_2$  annealing after the cPLD deposition, while samples B were exposed to the vapors of  $\text{CdCl}_2$  at  $360^\circ\text{C}$ , and they were fabricated with different durations of  $\text{CdCl}_2$  annealing 10, 12, 15, and 17 minutes corresponding to samples B1, B2, B3, and B4, respectively, as mentioned previously. Table 2 and Figure 5 show the highest efficiencies of the five samples and indicate that the best performance has been obtained at 15 minutes  $\text{CdCl}_2$  treatment for all thicknesses. Therefore, comparisons



TABLE 1: (a) Thicknesses and electrical properties of sample A without  $\text{CdCl}_2$  annealing. (b) Thicknesses and electrical properties of sample B3 with 15 min.  $\text{CdCl}_2$  annealing.

(a)				
Sample A	Layer 1	Layer 2	Layer 3	Layer 4
Thickness of CdS ( $\mu\text{m}$ )	0.12	0.12	0.12	0.12
Thickness of CdTe ( $\mu\text{m}$ )	1.5	1.25	1	0.75
$V_{\text{OC}}$ (mV)	214	198	203	197
$J_{\text{SC}}$ ( $\text{mA}/\text{cm}^2$ )	1.7	2.5	2.6	3.0
FF (%)	27	28	29	29
Efficiencies (%)	0.10	0.14	0.15	0.18
(b)				
Sample B3	Layer 1	Layer 2	Layer 3	Layer 4
Thickness of CdS ( $\mu\text{m}$ )	0.12	0.12	0.12	0.12
Thickness of CdTe ( $\mu\text{m}$ )	1.5	1.25	1	0.75
$V_{\text{OC}}$ (mV)	638	639	645	651
$J_{\text{SC}}$ ( $\text{mA}/\text{cm}^2$ )	16.5	16.7	17.0	18.0
FF (%)	36	39	42	45
Efficiencies (%)	4.0	4.2	4.6	5.1

TABLE 2: Efficiencies for five samples processed at different  $\text{CdCl}_2$  annealing times.

Layer thickness	No $\text{CdCl}_2$	10 min.	12 min.	15 min.	17 min.
Layer 1 (1.5 $\mu\text{m}$ )	0.08	1.73	2.39	4.46	2.90
Layer 2 (1.25 $\mu\text{m}$ )	0.12	1.95	4.35	4.79	3.51
Layer 3 (1.0 $\mu\text{m}$ )	0.13	2.30	4.54	5.09	3.99
Layer 4 (0.75 $\mu\text{m}$ )	0.15	2.95	5.16	5.34	4.08

of physical properties are made between samples A and B to elucidate the effect of the annealing on the solar cells with variable thicknesses of CdTe.

Figure 6 shows the key parameters of the solar cells as a function of thickness. The  $V_{\text{OC}}$  is essentially unchanged regardless of the CdTe thickness indicating that the same or comparable charge doping level, and thus the built-in bias voltage, was achieved in all layers. The  $J_{\text{SC}}$  values are also nearly identical between the layers of different thickness regardless of whether they were processed with or without the  $\text{CdCl}_2$  annealing. However, at least a sixfold increase in the  $J_{\text{SC}}$  value was observed in all layers in samples with  $\text{CdCl}_2$  annealing with respect to their counterparts without such annealing. The biggest factor contributing to differences in performance between layers was the FF. There is a linear decrease in FF observed with increasing CdTe thickness. The higher FF values seen at smaller CdTe thicknesses indicate the benefit of less recombination at smaller CdTe thickness as expected.

The efficiency of the solar cell can be further characterized by measuring the external quantum efficiency EQE, which represents the ratio between the numbers of electrons collected by the solar cell to the number of photons incidents on the solar cell [22]. Figure 7 shows the extreme difference in the EQE between samples A and B3 and allows us to gain

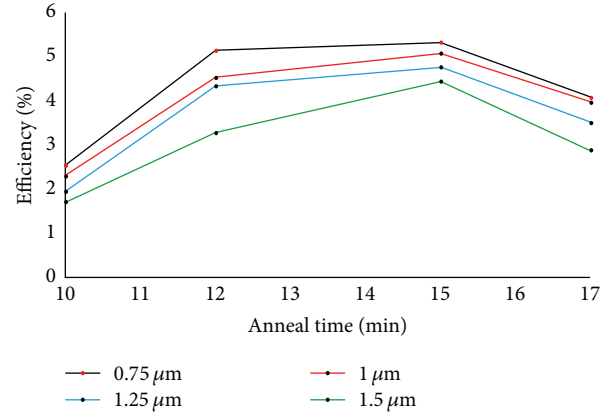


FIGURE 5: Plot of maximum solar cell efficiency versus  $\text{CdCl}_2$  anneal time, which were all obtained at a CdTe thickness of 0.75  $\mu\text{m}$ .

more insight into the behavior between the different CdTe thicknesses. The two thickest CdTe layers in sample B3 have nearly identical EQE curves implying that the recombination relative to CdTe thickness is the same for these two layers. When reducing the CdTe thickness from 1.25  $\mu\text{m}$  to 1  $\mu\text{m}$  an improvement in EQE was observed. An even further increase in EQE was observed when reducing the thickness by another 250 nm to 0.75  $\mu\text{m}$ . The entire increase in collection efficiency from layer 3 to layer 4 happens above the CdS band edge. This observation combined with the comparable grain size analysis for these two layers clearly indicates that the thinnest layer is the better performer because of less recombination in the CdTe due to the decreased number of grain boundaries encountered by electrons/holes in this cell.

## 4. Conclusion

CdTe/CdS thin-film solar cells with variable CdTe thickness in the range of 0.75  $\mu\text{m}$  to 1.5  $\mu\text{m}$  on the same sample were fabricated using a cPLD system. This combinatorial approach of device fabrication has allowed for an expedited optimization of the CdTe microstructure, crystallinity, and CdS/CdTe heterojunction in  $\text{CdCl}_2$  annealing. The grain size of the CdTe was found dependent on its thickness and an average grain size of  $\sim 450$  nm in the cPLD CdTe yields the best power conversion efficiency (5.3%) in the solar cells of the thinnest CdTe layer of 0.75  $\mu\text{m}$ , most probably due to the benefit of reduced charge recombination outweighing the reduced optical absorption. The cPLD method provides an efficient approach for exploration of device structures and can be used to further optimize these devices by changing a variety of PLD and CdTe/CdS solar cell parameters on the same device as well as allowing for quick exploration of devices with more complex cell structures.

## Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

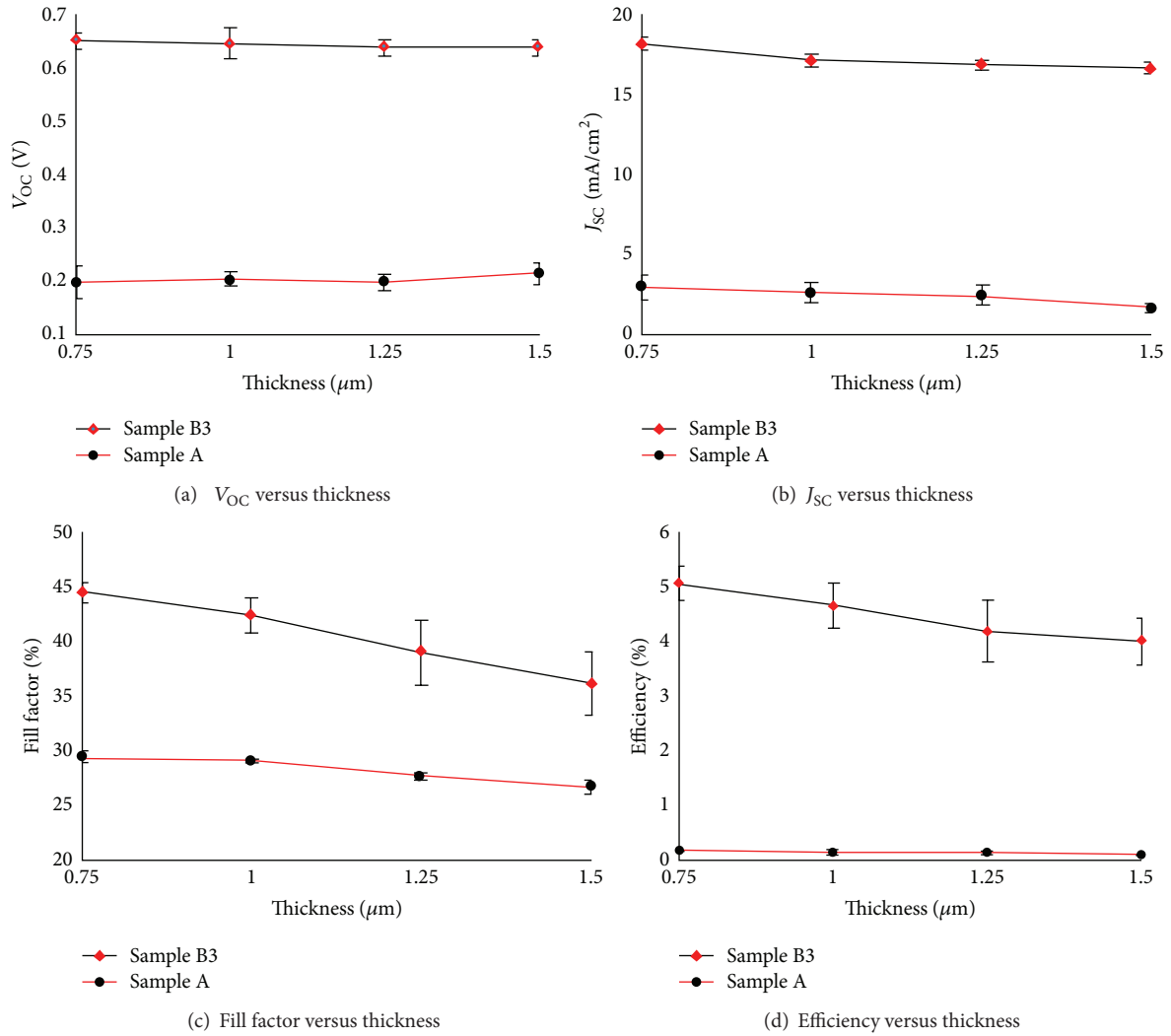


FIGURE 6: The values of open circuit voltage (a), short circuit current (b), fill factor (c), and efficiency (d) as a function of CdTe thickness for sample A made without any  $\text{CdCl}_2$  annealing and sample B3 that underwent a 15 min  $\text{CdCl}_2$  annealing.

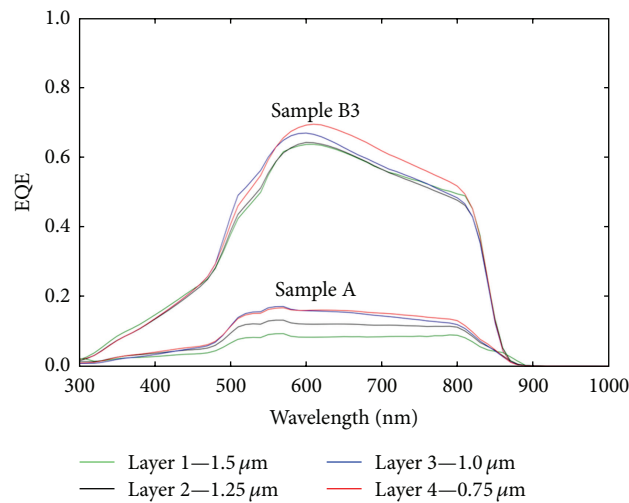


FIGURE 7: The quantum efficiencies for the best performing cells from the CdS/CdTe solar cells made without (sample A) and with (sample B3)  $\text{CdCl}_2$  annealing at  $360^\circ\text{C}$  for 15 min.

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